

Real Time Reconfiguration and Multi-Level Control for Microgrid

Anurag K Srivastava, Ramon Zamora, Farshid Shariatzadeh
 Smart Grid Demonstration and Research Investigation Lab (SGDRIL)
 The School of Electrical Engineering and Computer Science
 Washington State University

Motivation

- To maintain the availability of energy to the connected loads and to interrupt the smallest portion of the microgrid under any abnormal conditions
- To minimize problems due to relatively slow reconfiguration algorithms that cannot overcome real-time dynamics following any disturbance/fault
- To improve power system reliability for sensitive loads by better multi-level control mechanism for different operating scenarios
- To optimize renewable energy and local power resources to supply local load demand

Objectives

- To design a reconfiguration algorithm that can provides solution to maintain power to key loads
- To validate developed reconfiguration algorithms in real time before implementation using hardware in the loop setup and commercial automation controllers
- To model a microgrid that consists of DER as well as sensitive and non-sensitive loads
- To design controller that can regulate power sharing among DGs in an islanded and connected microgrid
- To design controller that can manage power exchange between grid and microgrid as well as among adjacent microgrids

Real-Time Reconfiguration of Microgrid

Intelligent Reconfiguration Algorithm (IRA)

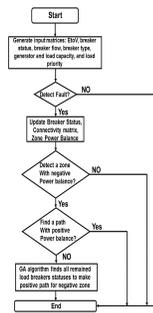
- Using graph theory and genetic algorithm
- Graph Theory
 - Model system and utilizes required matrices
- GA
 - Find optimal solution for breaker status in order to maximize served load w.r.t. load priority

➢ Components of power system are elements of graph representation

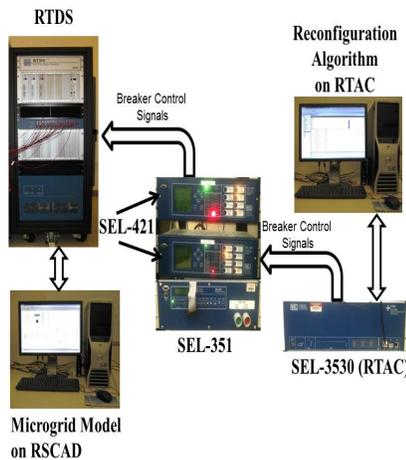
- Vertex of graph
 - Generator - Load - Cable - Bus
- Edge of graph
 - Circuit Breaker

- Fitness Function for GA
 - λ_{M_i} is priority for i^{th} load
 - x_i is i^{th} load CB status
 - P_{L_i} is power served to i^{th} load

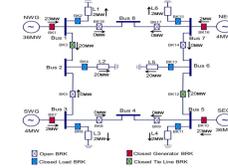
$$\text{Maximize } f(x) = \sum_{i=1}^n \lambda_{M_i} x_i P_{L_i}$$



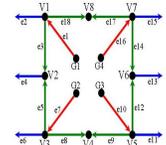
Hardware Setup



8-BUS System



Graph Representation



Real-Time Result

Test case	Faulted Bus Number	Negative power bus	Possible power supply path	Load Shedding	Breaker reconfiguration	MW Served
Case1	B1	B2	B2-B3-B4-B5-B6-B7-B8	L4	BK 11, 1, 2, 3, 18 (O) BK 5, 8, 9, 14 (C)	44
Case4	B1, B7	B2	B2-B3-B4-B5-B6	L3, L4	BK 1, 2, 3, 18, 17, 14, 15, 16, 11 (O) BK 5, 8, 9, 14 (C)	40

Multi-Level Control for Multiple Microgrids

Algorithm

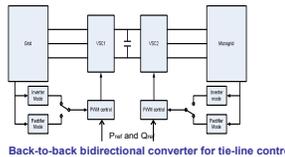
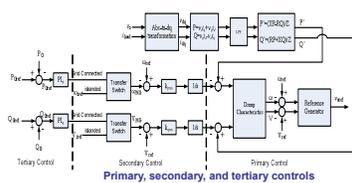
Multi-Level Control of Microgrid

Level 0 (inner loops):	Level 1 (primary):	Level 2 (secondary):	Level 3 (tertiary):
- Internal current loop - External voltage loop (PI and PWM)	- Power sharing among DGs (Droop and PI)	- Voltage magnitude and frequency restoration - Synchronization (PI)	- Power exchange between grid and microgrid or among adjacent microgrids (PI and MAS)

Example of Simulated Scenario

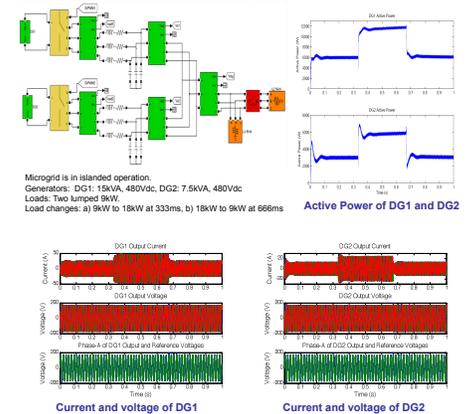
Islanded	Power sharing among DGs	Level 1 control
Grid-connected	Power exchange between grid and microgrid	Level 3 control
Transition	Seamless transition between grid-connected and islanded operation	Level 2 control (Synchronization)
Multiple microgrids	Power sharing among adjacent microgrids	Level 3 control

Control implementation



Note: Pref and Qref are from DMS or MMS or manually set

Example of Simulation Results



Summary

- Reconfiguration algorithm is fast enough in real-time to maintain maximum load under all possible conditions
- IRA can handle multi-objective functions and successfully implemented in real-time
- Droop control can share power between two parallel DGs based on their rated powers and local measurement only.

References

- [1] F. Shariatzadeh, R. Zamora, and A. K. Srivastava, "Real Time Implementation of Microgrid Reconfiguration," presented at 2011 North American Power Symposium, Boston, MA, Aug. 2011.
- [2] J.M. Guerrero, J.C. Vasquez, J. Matas, L.G. de Vicuña, and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158-172, Jan. 2011.

Acknowledgements:

